

## Xilinx CPLD Essentials:

This course consists of 2 packaged courses including:

- Fundamentals of CPLD Design (1 Day)
- Designing for Performance for CPLDs (1 Day)

## Fundamentals of CPLD Design

This comprehensive course provides you with an introduction to designing with Xilinx CPLDs. You will learn the basics of ISE software flow and how to interpret CPLD reports for optimum performance designs.

This course covers ISE features such as the Constraints Editor and PACE. Other topics are design planning, implementation options, and global timing constraints.

**Who Should Attend?** – Digital designers who have working knowledge of basic HDL (VHDL or Verilog) and who are new to Xilinx CPLDs, ISE software, or both

### Prerequisites

- Basic HDL knowledge (VHDL or Verilog)
- Digital design experience

### Recommended Hardware Demo Board

- Coolrunner™-II Starter Kit (part number HW-CR11-SK-G)
  - Not used in the online course

After completing this comprehensive training, you will have the necessary skills to:

- Describe what products Xilinx offers and where the CoolRunner-II CPLD fits into this offering
- Identify the basic architectural resources of the CoolRunner-II CPLD
- Describe the CPLD tool flow: Design entry, synthesis, implementation, and programming
- Specify global timing constraints and pin assignments
- Access and implement basic and advanced CPLD software options via the ISE software

## Course Outline

- Course Agenda
- Introduction to Xilinx Products
- CoolRunner-II CPLD Architecture
- CPLD Software Flow
- **Lab 1:** Xilinx CPLD Tool Flow
- Reading CPLD Reports
- Global Constraints
- **Lab 2:** Constraints for CPLDs
- CPLD Software Options
- **Lab 3:** CPLD Implementation Options

## Lab Descriptions

- **Lab 1:** Xilinx CPLD Tool Flow – Create a new project in the Project Navigator of the ISE software. Implement a design by using default software options and configure the CoolRunner-II CPLD demo board with iMPACT, the Xilinx In-System Programming (ISP) software.
- **Lab 2:** Constraints for CPLDs – Use constraints to specify clock frequencies, pin locations, and I/O standards for the CPLD demo board project. Fit the design and analyze the Timing and Fitter Reports to confirm performance and I/O placement.
- **Lab 3:** CPLD Implementation Options – Implement the design with default software options and evaluate the design performance versus design requirements. Apply a global timing constraint for PERIOD to the design. Change the software options and add I/O constraints to meet the design's timing goals.

## Designing for Performance, CPLDs

*Designing for Performance for CPLDs* is an intermediate-level course that provides a comprehensive overview of the CPLD software flow. By applying the techniques presented in this course, you will be able to enhance design performance and make the best possible use of Xilinx CPLD architectures.

This course uses the ISE™ software, including the Constraints Editor & Timing Analyzer. Other topics include understanding the CPLD logic engine, estimating power, and fitting difficult designs.

**Who Should Attend?** – Digital designers who have working knowledge of basic HDL (VHDL or Verilog) and who have some experience designing with Xilinx CPLDs. Alternatively, those who have recently attended *Fundamentals of CPLD Design*.

### Prerequisites

- Basic HDL knowledge (VHDL or Verilog)
- Digital design knowledge and Xilinx CPLD experience
- *Fundamentals of CPLD Design* course or equivalent knowledge of CPLD architecture; Xilinx implementation software flow and options; global constraints, the Constraints Editor; and reading fitting and timing reports
- Some experience with the software tool flow and global timing constraints

After completing this comprehensive training, you will have the necessary skills to:

- Apply techniques to fit more logic into a device
- Describe the CoolRunner™-II CPLD timing model and how it can be used to analyze design performance
- Describe the advanced capabilities of the CoolRunner-II CPLD architecture
- Estimate the power consumption of a CPLD design

## Course Outline

- Course Agenda
- Review of Fundamentals of CPLD Design
- XST for CPLDs
- Advanced Fitting
- Handling No-Fit Situations
- **Lab 1:** Fitting
- CPLD Timing
- **Lab 2:** CPLD Timing
- CPLD Logic Engine
- Coding Techniques
- CPLD Best Design Practices
- Power Estimation

## Lab Descriptions

- **Lab 1:** Fitting – Apply the knowledge and techniques learned in the previous modules to fit designs into smaller devices.
- **Lab 2:** CPLD Timing – Analyze the timing of a design and create testbenches that can be simulated to verify the behavior of the design.

## Register Today

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