

Course Description

As FPGA designs become increasingly more complex, designers continue to look to reduce design and debug time. The powerful, yet easy-to-use ChipScope™ Pro tool solution helps minimize the amount of time required for verification and debug.

This two-day course will not only introduce you to the cores and tools and illustrate how to use the triggers effectively, but also show you effective ways to debug logic and high-speed designs—thereby decreasing your overall design development time. This training will provide hands-on labs that demonstrate how the ChipScope Pro tools can address advanced verification and debugging challenges.

Course Duration – 2 day

Who Should Attend? – System and logic designers who want to minimize verification and debug time

Prerequisites

- Basic language concepts for both days
 - Designing with VHDL* or equivalent knowledge of VHDL
 - Designing with Verilog* or equivalent knowledge of Verilog
- Basic FPGA skills for Day 1
 - Essentials of FPGA Design*
- Intermediate FPGA skills for Day 2
 - Designing for Performance*
- ChipScope Pro Software REL strongly recommended (www.xilinx.com/support/training/rel/chipscopepro-rel.htm)

Software Tools

- Xilinx ISE® Design Suite: Logic or System Edition 12.1
- ChipScope Pro 12.1 software

Hardware

- Demo board: Spartan-6 FPGA SP605 board

After completing this comprehensive training, you will have the necessary skills to:

- Identify each ChipScope Pro tool core and explain its purpose
- Effectively utilize the ChipScope Pro Analyzer tool
- Implement the ChipScope Pro tool using the CORE Generator™, Core Inserter, and PlanAhead™ tool flows
- Select effective test points in your design
- Optimize design and core performance when ChipScope Pro tool cores are used
- Execute various techniques for collecting data, including file storage, scripting, and building custom triggers

Course Outline

Day 1

- How the ChipScope Pro Tool Works
- Inserting the Cores – Inserter Flows: Core Inserter and the PlanAhead Software
- Labs 1a and 1b:** Using the Inserter Tool from Project Navigator and Using the Inserter Tool from the PlanAhead software
- Instantiating the Cores – The CORE Generator Tool Flow
- Lab 2:** Using the CORE Generator Tool from Project Navigator
- Triggering and Storage
- Visualizing Data – The ChipScope Pro Analyzer Tool
- Lab 3:** Triggering and Visualization in the Analyzer Tool

Day 2

- Tips and Tricks
- Lab 4:** Tips and Tricks

- Time for Timing
- Video Demo – Area Groups for Isolation
- Case Studies
- Lab 5:** FPGA Editor Support for the ChipScope Pro Tool
- Scripting (Optional)*
- Lab 6:** VIO Tcl Scripting (Optional)*
- Remote Access (Optional)*
- Lab 7:** Remote Access (Optional)*

* Check with us which content is included with your specific class.

Lab Descriptions

- Labs 1a and 1b:** Using the Inserter Tool from Project Navigator (Lab 1a) and Using the Inserter Tool from the PlanAhead Software (Lab 1b) – Insert an ICON and ILA cores into an existing netlist and debug a common problem.
- Lab 2:** Using the CORE Generator Tool from Project Navigator – Build upon a provided design to create and instantiate a VIO core and observe its behavior using the ChipScope Pro Analyzer tool.
- Lab 3:** Triggering and Visualization in the Analyzer Tool – Configure triggers and view captured data using the ChipScope Pro Analyzer tool.
- Lab 4:** Tips and Tricks – Keep time across multiple sample windows; sample across multiple time domains; and implement a complex custom (unconventional) trigger.
- Lab 5:** FPGA Editor Support for the ChipScope Pro Tool – Change the signals being sampled by an ILA without having to reimplement the design.
- Lab 6:** VIO Tcl Scripting – Configure automated analysis.
- Lab 7:** Remote Access – Use the ChipScope Pro Analyzer tool to configure an FPGA, set up triggering, and view the sampled data from a remote location.

Register Today

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