

Live Online Instructor Led Training

Online courses can be broken in to sessions, normally 3-4hrs long, over several weeks, depending on the attendees' requirements. For that reason we also state the course length in hours, removing lunch breaks. Labs can also be done in your own time between sessions if desired, but your lecturer will always assign time to stay online while you do the labs should you so wish. Basically we try to have as much flexibility as possible to best fit the class requirements.

Xilinx Designing with Verilog:

This comprehensive course is a thorough introduction to the Verilog language. The emphasis is on writing Register Transfer Level (RTL) and behavioral source code. This class addresses targeting Xilinx devices specifically and FPGA devices in general. The information gained can be applied to any digital design by using a top-down synthesis design approach. This course combines insightful lectures with practical lab exercises to reinforce key concepts. You will also learn advanced coding techniques that will increase your overall Verilog proficiency and enhance your FPGA optimization. This course covers Verilog 1995 and 2001.

In this three-day course, you will gain valuable hands-on experience. Incoming students with little or no Verilog knowledge will finish this course empowered with the ability to write efficient hardware designs and perform high-level HDL simulations.

Course Duration – 3 days / ~20hrs
Price – AU\$1485. Tax free / outside of Australia
Who Should Attend? – Engineers who want to use Verilog effectively for modeling, design, and synthesis of digital designs
Prerequisites

- Basic digital design knowledge

Software Tools

- Xilinx ISE® Design Suite: Logic or System Edition 13.1

Hardware

- Architecture: N/A*
- Demo board: Spartan®-6 FPGA SP605 board*

After completing this comprehensive training, you will have the necessary skills to:

- Write RTL Verilog code for synthesis
- Write Verilog test fixtures for simulation
- Create a Finite State Machine (FSM) by using Verilog
- Target and optimize Xilinx FPGAs by using Verilog
- Use enhanced Verilog file I/O capability
- Run a timing simulation by using Xilinx Simprim libraries
- Create and manage designs within the ISE software design environment
- Download to the Spartan-6 FPGA SP605 demo board

Course Outline

Day 1

- Hardware Modeling Overview
- Verilog Language Concepts
- Modules and Ports
- Lab 1:** Building Hierarchy
- Introduction to Testbenches
- Lab 2:** Verilog Simulation and RTL Verification

Day 2

- Verilog Operators and Expressions
- Data Flow-Level Modeling
- Lab 3:** Memory
- Verilog Procedural Statements
- Lab 4:** Clock Divider and Address Counter
- Controlled Operation Statements
- Lab 5:** n-bit Binary Counter and RTL Verification

Day 3

- Verilog Tasks and Functions
- Advanced Language Concepts
- Lab 6:** Timing Simulation
- Finite State Machines
- Lab 7:** Finite State Machines
- Targeting Xilinx FPGAs
- Lab 8:** Implement and Download
- Advanced Verilog Testbenches
- Lab 9:** Using Verilog File I/O

Lab Descriptions

The labs for this course provide a practical foundation for creating synthesizable RTL code. All aspects of the design flow are covered in the labs. The labs are written, synthesized, behaviorally simulated, and implemented by the student. The focus of the labs is to write code that will optimally infer reliable and high-performance circuits. The labs culminate in a functional calculator that students verify in simulation.

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the Logic Portal

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