

Live Online Instructor Led Training

Online courses can be broken in to sessions over several weeks, depending on the attendees' requirements. For that reason we also state the course length in hours, removing lunch breaks. Usually we run the course over 8 -10, 3-4hr sessions. Labs can also be done in your own time between sessions if desired, but your lecturer will always assign time to stay online while you do the labs should you so wish. Basically we try to have as much flexibility as possible to best fit the classes requirements.

Xilinx Academy I Description:

The Academy I course consists of 3 packaged courses including:

- ISE Design Entry – 6.5 hours (1 day)
- Designing with VHDL or Verilog – 20 hours (3 days)
- Essentials of FPGA Design – 6.5 hours (1 day)

Full course: AU\$2295. Tax only applies to Australian companies. Individual days are AU\$495

A Digilent Demo Board may be purchased with an Academic discount when attending this course. See the end of this brochure for details.

ISE Design Entry

ISE Design Tool Flow provides the overall context and framework for the development cycle of FPGAs. This course will arm you with a project planning techniques strategy, and go through the FPGA tool flow to get up and designing an FPGA design now.

The flow will take you from behavioral specification to tuning specifications for the FPGA, synthesis, verification, and onto implementation and download. Throughout the design cycle, the various tools within the Project Navigator tool are introduced.

Who Should Attend? – Digital designers new to FPGA design who need to learn the FPGA design cycle and the major aspects of the ISE® 13.1 design tools

Prerequisites

- None. Any digital knowledge and VHDL/Verilog skills useful

Recommended RELs*

- Basic FPGA Architecture: Slice and I/O Resources
- Basic FPGA Architecture: Memory and Clocking Resources

Hardware

- Architecture: Spartan®-6 and Virtex®-6 FPGAs
- Demo board: None

* Go to www.xilinx.com/education and click View Training Modules link

After completing this comprehensive training, you will have the necessary skills to:

- Outline a complete project planning process
- Create a new Project Navigator project in the ISE software
- Access and modify Xilinx Synthesis Technology (XST) synthesis options
- Assign pin locations using the I/O PlannerEnter global clock constraints using the Xilinx Constraints Editor

Course Specification

- Simulate a design using the ISim Simulator

Course Outline

- Course Agenda
- Project Planning
- Projects in the Project Navigator
- **Lab 1:** Projects in the Project Navigator
- HDL Synthesis and XST
- **Lab 2:** XST Synthesis Options
- Constraints and the I/O Planner
- **Lab 3:** I/O Pin Planning
- ISim Simulator
- **Lab 4:** ISim Simulator
- Additional Features
- Summary

Lab Descriptions

- **Lab 1:** Projects in the Project Navigator – Gain comprehensive hands-on experience with the HDL flow in the ISE software. Create a new project, add source files, synthesize a design, and use the error navigation feature to fix your HDL code.
- **Lab 2:** Synthesis Options – Modify XST synthesis properties, read synthesis reports to compare the synthesis results with the implemented results, and use the schematic viewer to evaluate the design.
- **Lab 3:** I/O Pin Planning – Review demo board documentation to determine the finished pinout and use the PlanAhead™ tool to assign pin location constraints and set other pin attributes.
- **Lab 4:** ISim Simulator – Use the project navigator to view an HDL testbench, use the ISim Simulator to run simulation view output waveforms, add signals, and change their viewed format.

Designing with VHDL or Verilog

Please see the Verilog course summary here:

<http://www.thelogicportal.com/wp-content/uploads/Designing-with-Verilog-Online.pdf>

This comprehensive course is a thorough introduction to the VHDL language. The emphasis is on writing solid synthesizable code and enough simulation code to write a viable testbench. Structural, Register Transfer Level (RTL), and behavioral coding styles are covered. This class addresses targeting Xilinx devices specifically and FPGA devices in general. The information gained can be applied to any digital design by using a top-down synthesis design approach.

This course combines insightful lectures with practical lab exercises to reinforce key concepts. You will also learn best coding practices that will increase your overall VHDL proficiency.

Who Should Attend? – Engineers who want to use VHDL effectively for modeling, design, and synthesis of digital designs

Prerequisites

- Basic digital design knowledge

Hardware

- Demo board: None

- Implement the VHDL portion of coding for synthesis
 - Identify the differences between behavioral and structural coding styles
 - Distinguish coding for synthesis versus coding for simulation
 - Use scalar and composite data types to represent information
 - Use concurrent and sequential control structure to regulate information flow
 - Implement common VHDL constructs (Finite State Machines [FSMs], RAM/ROM data structures)
- Simulate a basic VHDL design
 - Write a VHDL testbench and identify simulation-only constructs
- Identify and implement coding best practices
 - Optimize VHDL code to target specific silicon resources within the Xilinx FPGA
- Create and manage designs within the ISE software environment

Course Outline

Day 1

- The “Shape” of VHDL
- **Lab 1:** Using the Tools
- Documentation in VHDL
- Data Types
- Concurrent Operations
- **Lab 2:** Using Concurrent Statements
- Processes and Variables
- **Lab 3:** Designing a Simple Process

Day 2

- Introduction to Testbenches
- ISim Simulation Tool Basics
- **Lab 4:** Simulating a Simple Design
- Creating Memory
- **Lab 5:** Building a Dual-Port Memory
- Finite State Machines
- **Lab 6:** Building a Moore Finite State Machine
- Targeting Xilinx FPGAs
- **Lab 7:** Simple 4-bit ALU

Day 3

- Loops and Conditional Elaboration
- **Lab 8:** Using Loops
- Attributes
- Functions and Procedures
- Packages and Libraries
- **Lab 9:** Building Your Own Package
- Interacting with the Simulation
- Writing a Good Testbench
- **Optional Lab 10:** Building a Meaningful Testbench

Labs Description

The labs for this course provide a practical foundation for creating synthesizable RTL code. All aspects of the design flow are covered in the labs. You will write, synthesize, simulate, and implement all the labs. The focus of the labs is to write code that will optimally infer reliable and high-performance circuits.

Essentials of FPGA Design

Use the ISE[®] software tools to implement a design and gain an understanding of the Essential Xilinx FPGA architecture. Understand best design practices for synchronous, reliable design from the pros as well as the subtleties of the Xilinx design flow.

This course covers ISE software features such as the Architecture Wizard, I/O Planner, and the Constraints Editor. Other topics include FPGA architecture, good design practices, understanding report contents, and the PERIOD and OFFSET global timing constraints.

For more emphasis on improving the overall design performance, take the follow-up course *Designing for Performance*, which builds on the basic principles covered in this course.

* Go to www.xilinx.com/education and click the Recorded e-Learning link to view these RELs.

Who Should Attend? – Designers who are new to Xilinx FPGAs Recommended RELs

- Architecture Wizard and I/O Planning REL*

Prerequisites

- Basic working HDL knowledge (VHDL or Verilog) useful
- Digital design experience very useful

Other Optional RELs

- Basic HDL Coding Techniques REL* (parts 1 and 2)
- Virtex-6 and Spartan-6 FPGA HDL Coding Techniques REL*

Hardware

- Architecture: Spartan[®]-6 FPGA**
- Demo board: Spartan-6 FPGA SP605 or Virtex-6 FPGA ML605

After completing this comprehensive training, you will have the necessary skills to:

- Take advantage of the primary features of the Spartan-6 FPGA
- Use the Project Navigator to implement and simulate a design
- Read reports and determine whether your design goals were met
- Use the Clocking Wizard to create DCM instantiations
- Use the I/O Planner to make good pin assignments
- Use the Xilinx Constraints Editor to enter global timing constraints

Course Outline

- Course Agenda
- Basic FPGA Architecture
- Xilinx Tool Flow
- **Optional Lab 1:** Xilinx Tool Flow – **You will need an SP605 board to download or otherwise bypass this small section.**
- Reading Reports
- **Lab 2:** Clocking Wizard and Pin Assignment
- **Lab 3:** Pre-Assigning I/O Pins Using the PlanAhead Tool
- Global Timing Constraints
- **Lab 4:** Global Timing Constraints
- Synchronous Design Techniques
- Course Summary

Lab Descriptions

- **Lab 1:** Xilinx Tool Flow – Create a new project in the ISE Project Navigator and use the ISE Simulator to perform a behavioral simulation. Implement the design using default software options and download to a Spartan-6 FPGA SP605 evaluation board.

Version 13.1 – 2011 – Using ISE 13.1

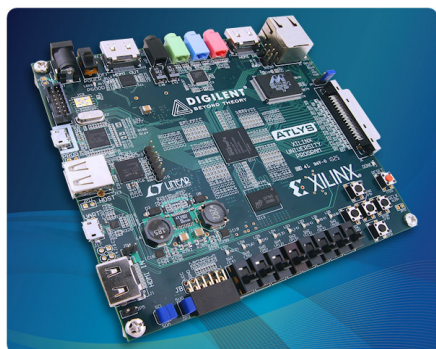
- **Lab 2:** Clocking Wizard and Pin Assignment – Use the Clocking Wizard to customize a DCM and incorporate your clocking resources into your design. Use the PlanAhead™ tool to assign pin locations and implement the design using the Project Navigator in the ISE software.
- **Lab 3:** Pre-Assigning I/O Pins Using the PlanAhead Tool – This lab introduces the basics of making good I/O pin assignments with the PlanAhead software. Use the Design Rule Checker to follow the I/O banking rules.
- **Lab 4:** Global Timing Constraints – Enter global timing constraints with the Xilinx Constraints Editor. Review the Post-Map Static Timing Report to verify that the timing constraints are realistic. Use the Post-Place & Route Static Timing Report to determine the delay of the longest constrained path for each timing constraint.

Purchase a Digilent board at Academic pricing when you attend this course.

Please add Tax inside Australia. Pricing correct at time of print, up to date pricing can be found on our online shop.

There are many boards available which can be discounted as part of attending this course. We recommend the following boards. More details on the website.

Spartan-6 Atlys Board



Normal Pricing	AU\$399
Academy Price	AU\$235 - Big Savings!

Course Specification

Spartan-3E Starter Kit



Spartan-3E Starter Kit	500k
Normal Pricing	AU\$210
Academy Price	AU\$189

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