

Live Online Instructor Led Training

Online courses can be broken in to sessions over several weeks, depending on the attendees' requirements. For that reason we also state the course length in hours, removing lunch breaks. Usually we run the course over 8 -10, 3-4hr sessions. Labs can also be done in your own time between sessions if desired, but your lecturer will always assign time to stay online while you do the labs should you so wish. Basically we try to have as much flexibility as possible to best fit the class's requirements.

Xilinx Academy II Description:

The Academy II course consists of 3 packaged courses including:

- Design Tips & Techniques for Low Cost – 13 hrs (2 days)
- Designing For Performance - 13 hrs (2 days)
- Debugging Techniques Using Chipscope Part 1- 6.5hrs (1 day)

Full course: AU\$2295. Tax only applies to Australian companies. Individual days are AU\$495

A Diligent Demo Board may be purchased with an Academic discount when attending this course. See the end of this brochure for details.

Design Tips & Techniques

This is one of our favorite courses, with consistently good feedback. This course appeals to engineers who have an interest in good design techniques, to produce compact design (for lower cost) with additional discussion on timing performance. The course and exercises cover several different design techniques, which will be interesting and challenging for any digital designer regardless of the final application.

Level – Fundamental - Intermediate

Prerequisites

- An understanding of digital design and the concept of an FPGA
- An appreciation of VHDL is very beneficial

Supported Devices

- Spartan-6, Virtex - 6

After completing this comprehensive training, you will have the necessary skills to:

- Accurately estimate design size to aid in predicting product costs
- Apply design techniques that result in low-cost implementations
- Explore creative ways to use the FPGA , Slices, memory, and DSP resources to reduce design size and increase performance.

Course Outline

- Refresh: Why an FPGA?
- Spartan-6 & Virtex-6 overview
- Data and Control Pin Layout
- Understanding CLBs and Slices
- The LUT6
- Multiplexers
- Flip-Flops and Control Sets
- Reset Considerations
- Synchronous Timing vs. Asynchronous Timing
- Digital Clock Managers
- Number Representation

- Dedicated Carry Logic
- Counters
- Wired Carry Gates
- Block Memory
- Distributed RAM
- FIFO
- Dual Port Memory
- State Machines
- DSP48 for General Logic Usage

Exercises

- 6 input LUT Functions
- Logic Levels
- Multiplexers using LUTs
- Dedicated Multiplexers
- Flip Flop Controls
- Performance by Design
- Clocks
- Counters
- Fractional Number Formats
- Adders
- Wired Carry Gates
- Aspect Ratios
- Replacing Logic With Block RAM
- Distributed RAM
- Essence of FIFOs
- Delays
- State Machines
- DSP48 OPCODE's

Designing for Performance

Attending the *Designing for Performance* class will help you create more efficient designs. This course can help you fit your design into a smaller FPGA or a lower speed grade for reducing system costs. In addition, by mastering the tools and the design methodologies presented in this course, you will be able to create your design faster, shorten your development time, and lower development costs.

Who Should Attend? – FPGA designers with intermediate knowledge of HDL and some experience with the Xilinx ISE® software tools

Prerequisites

- *Essentials of FPGA Design* course or equivalent knowledge of FPGA architecture features; the Xilinx implementation software flow and implementation options; reading timing reports; basic FPGA design techniques; global timing constraints and the Constraints Editor
- Intermediate HDL knowledge (VHDL or Verilog)
- Solid digital design background

Recommended RELs

- Basic HDL Coding Techniques REL (parts 1 and 2)
- Virtex-6 & Spartan-6 FPGA HDL Coding Techniques RELs
- Power Estimation REL

Hardware

- Architecture: Spartan®-6 and Virtex-6 FPGAs*
- Demo board: Spartan-6 FPGA SP605 board*

Version 13.1 Using ISE 13.1 Software

After completing this comprehensive training, you will have the necessary skills to:

- Describe the architectural features of the Virtex-6 FPGA and Spartan-6 FPGAs
- Identify the different members of the 7 series families
- Create and integrate cores into your design flow by using the CORE Generator™ interface
- Describe the clocking features of the Virtex-6 and Spartan-6 FPGAs and how they can be used to improve performance
- Increase performance by duplicating registers and pipelining
- Increase system reliability by adding an appropriate synchronization circuit
- Describe different synthesis options and how they can improve performance
- Describe a flow for obtaining timing closure
- Pinpoint design bottlenecks by using Timing Analyzer reports
- Apply advanced timing constraints to meet your performance goals
- Use advanced implementation options to increase design performance

Course Outline

Day 1

- Review of *Essentials of FPGA Design*
- Designing with FPGA Resources
- CORE Generator Software System
- Basic FPGA Clock Resources
- Virtex-6 and Spartan-6 FPGA Clock Resources
- Lab 1:** Designing With FPGA Resources
- FPGA Design Techniques
- Synthesis Techniques
- Lab 2:** Synthesis Techniques

Day 2

- Achieving Timing Closure
- Lab 3:** Review of Global Timing Constraints
- Path-Specific Timing Constraints, Part 1
- Path-Specific Timing Constraints, Part 2
- Lab 4:** Achieving Timing Closure
- Advanced Implementation Options
- Lab 5:** Designing for Performance
- Lab 6:** FPGA Editor Demo (optional)
- ChipScope Pro Software (optional)
- Lab 7:** ChipScope Pro Software (optional)

Lab Descriptions

- Lab 1:** Designing with FPGA Resources – Create block RAM and clocking FPGA cores using the CORE Generator™ tool. Instantiate these cores and other clock resources and implement the design.
- Lab 2:** Synthesis Techniques – Experiment with different synthesis options (including timing constraints, resource sharing, synthesis optimization effort, and register balancing) and view the results.
- Lab 3:** Review of Global Timing Constraints – Use the Constraints Editor to enter global timing constraints.

Course Specification

- Lab 4:** Achieving Timing Closure – Review timing reports and enter path-specific timing constraints to fully describe your performance requirements.
- Lab 5:** Designing for Performance – Improve performance and maximize results solely with implementation options and SmartXplorer.
- Lab 6:** FPGA Editor Demo (optional) – Use the FPGA Editor to view a design and add a probe to an internal net.
- Optional: Lab 7:** ChipScope Pro Software (optional) – Add an internal logic analyzer to a design to perform real-time debugging. **This lab requires both an SP605 Board and also a full version of the ISE tools. Chipscope is not included in Webpack, but can be purchased as an add-on.**

Debugging Techniques Using the ChipScope Pro Tools

This course module requires both an SP605 Board and also a full version of the ISE tools. Chipscope is not included in Webpack, but can be purchased as an add-on.

As FPGA designs become increasingly more complex, designers continue look to reduce design and debug time. The powerful, yet easy-to-use ChipScope™ Pro tool solution helps minimize the amount of time required for verification and debug.

Academy II covers day one of this two-day course (Day 2 is part of Academy III) which will introduce you to the cores and tools and illustrate how to use the triggers effectively, but also show you effective ways to debug logic and high-speed designs—thereby decreasing your overall design development time. This training will provide hands-on labs that demonstrate how the ChipScope Pro tools can address advanced verification and debugging challenges.

Who Should Attend? – System and logic designers who want to minimize verification and debug time

Prerequisites

- Basic language concepts for both days
- Designing with VHDL* or equivalent knowledge of VHDL
- Designing with Verilog* or equivalent knowledge of Verilog
- Basic FPGA skills for Day 1
- Essentials of FPGA Design*
- Intermediate FPGA skills for Day 2
- Designing for Performance*
- ChipScope Pro Software REL strongly recommended (www.xilinx.com/support/training/rel/chipscopepro-rel.htm)

Hardware

- Architecture: N/A*
- Demo board: Spartan-6 FPGA SP605 board

After completing this comprehensive training, you will have the necessary skills to:

- Identify each ChipScope Pro tool core and explain its purpose
- Effectively utilize the ChipScope Pro Analyzer tool
- Implement the ChipScope Pro tool using the CORE Generator™, Core Inserter, and PlanAhead™ tool flows
- Select effective test points in your design
- Execute various techniques for collecting data.

Course Outline

- How the ChipScope Pro Tool Works
- Inserting the Cores – Inserter Flows: Core Inserter and the PlanAhead Software
- Labs 1 and 2:** Using the Inserter Tool from Project Navigator and Using the Inserter Tool from the PlanAhead software
- Instantiating the Cores – The CORE Generator Tool Flow
- Lab 3:** Using the CORE Generator Tool from Project Navigator
- Triggering and Storage
- Visualizing Data – The ChipScope Pro Analyzer Tool
- Lab 4:** Triggering and Visualization in the Analyzer Tool

Lab Descriptions

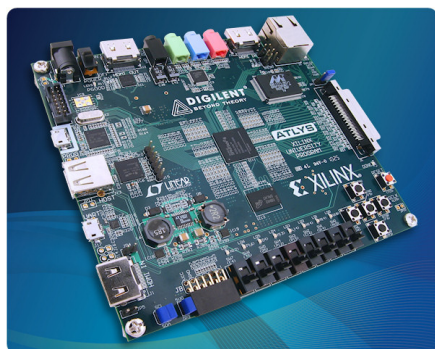
- Labs 1 and 2:** Using the Inserter Tool from Project Navigator (Lab 1) and Using the Inserter Tool from the PlanAhead Software (Lab 2) – Insert an ICON and ILA cores into an existing netlist and debug a common problem.
- Lab 3:** Using the CORE Generator Tool from Project Navigator – Build upon a provided design to create and instantiate a VIO core and observe its behavior using the ChipScope Pro Analyzer tool.
- Lab 4:** Triggering and Visualization in the Analyzer Tool – Configure triggers and view captured data using the ChipScope Pro Analyzer tool.

Purchase a Digilent board at Academic pricing when you attend this course.

Please add Tax inside Australia. Pricing correct at time of print, up to date pricing can be found on our online shop.

There are many boards available which can be discounted as part of attending this course. We recommend the following boards. More details on the website.

Spartan-6 Atlys Board



Normal Pricing	AU\$399
Academy Price	AU\$235 - Big Savings!

Spartan-3E Starter Kit



Spartan-3E Starter Kit	500k
Normal Pricing	AU\$210
Academy Price	AU\$189

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